From the INTERNATIONAL BUREAU

PCT

NOTIFICATION CONCERNING TRANSMITTAL OF COPY OF INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY (CHAPTER I OF THE PATENT COOPERATION TREATY)
(PCT Rule 44bis.1(c))

To:

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Date of mailing *(day/month/year)* 31 December 2008 (31.12.2008)	
Applicant's or agent's file reference 0057-026P1PCT	**IMPORTANT NOTICE**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2007/004082	16 February 2007 (16.02.2007)	16 February 2006 (16.02.2006)

Applicant
VNS PORTFOLIO LLC et al

The International Bureau transmits herewith a copy of the international preliminary report on patentability (Chapter I of the Patent Cooperation Treaty)

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PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44*bis*)

Applicant's or agent's file reference 0057-026P1PCT	**FOR FURTHER ACTION**	See item 4 below
International application No. PCT/US2007/004082	International filing date *(day/month/year)* 16 February 2007 (16.02.2007)	Priority date *(day/month/year)* 16 February 2006 (16.02.2006)
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant VNS PORTFOLIO LLC		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 *bis*.1(a).

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

   In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

   - ☒ Box No. I — Basis of the report
   - ☐ Box No. II — Priority
   - ☐ Box No. III — Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - ☐ Box No. IV — Lack of unity of invention
   - ☒ Box No. V — Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - ☐ Box No. VI — Certain documents cited
   - ☐ Box No. VII — Certain defects in the international application
   - ☐ Box No. VIII — Certain observations on the international application

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44*bis*.3(c) and 93*bis*.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44*bis* .2).

	Date of issuance of this report 16 December 2008 (16.12.2008)
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. +41 22 338 82 70	Authorized officer Nora Lindner e-mail: pt11.pct@wipo.int

Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
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CORRECTED

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	10 NOV 2008
Applicant's or agent's file reference 0057-026P1PCT	FOR FURTHER ACTION See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US 07/04082	16 February 2007 (16.02.2007)	16 February 2006 (16.02.2006)

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - G06F 9/46 (2008.04)
USPC - 718/100

Applicant VNS PORTFOLIO LLC

1. This opinion contains indications relating to the following items:

- [X] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [X] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	29 October 2008 (29.10.2008)	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (April 2007)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 07/04082

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:
   - [x] the international application in the language in which it was filed.
   - [ ] a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. [ ] This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:
   a. type of material
      - [ ] a sequence listing
      - [ ] table(s) related to the sequence listing
   b. format of material
      - [ ] on paper
      - [ ] in electronic form
   c. time of filing/furnishing
      - [ ] contained in the international application as filed
      - [ ] filed together with the international application in electronic form
      - [ ] furnished subsequently to this Authority for the purposes of search

4. [ ] In addition, in the case that more than one version or copy of a sequence listing and/or table(s) relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

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Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	none	YES
	Claims	1-38	NO
Inventive step (IS)	Claims	none	YES
	Claims	1-38	NO
Industrial applicability (IA)	Claims	1-38	YES
	Claims	none	NO

2. Citations and explanations:

Claims 1-38 lack novelty under PCT Article 33(2) as being anticipated by US 2005/0114565 A1 to Gonzalez et al. (hereinafter, 'Gonzalez').

Regarding claim 1, Gonzalez teaches a method for communicating between a plurality of computer processors, comprising: providing a first processor; providing a second processor (Fig. 1, para [0010]); and sending an input from said first processor to said second processor, wherein said sending does not cause an interrupt in processing functions of said second processor (information is communicated by message-passing among arrayed processor nodes, para [0060]).

Regarding claim 2, Gonzalez teaches wherein: said input comprises a write function from said first processor to said second processor (passing data by writing to a memory mapped interface, Fig. 2, para [0043]).

Regarding claim 3, Gonzalez teaches wherein: each of said plurality of processors comprises a plurality of communication ports (processor network interface 240 is a communication interface, Fig. 2, para [0041]).

Regarding claim 4, Gonzalez teaches wherein: each of said plurality of processors further comprises an input/output (I/O) register (processor network interface 240 passes data to or from a memory mapped interface to read or write, para [0043]).

Regarding claim 5, Gonzalez teaches wherein: each of said input/output (I/O) registers comprises read and write status bits (standard I/O communication signals are communication signals that conform to commonly accepted industry or company standards, protocols, conventions, technology, or circuitry, Fig. 9, para [0085]).

Regarding claim 6, Gonzalez teaches further comprising: a step of checking the status of said read and write status bits (standard I/O interface 914 is an interface configured to handle standard I/O communication signals between chips or devices, Fig. 9, para [0085]).

Regarding claim 7, Gonzalez teaches wherein: said plurality of processors comprises an array of processors provided on a die (the array of processor nodes 140 is implemented as a multiprocessor system-on-a-chip, Fig. 1, para [0035]).

Regarding claim 8, Gonzalez teaches wherein: said sending is provided via a data bus between said first processor and said second processor (processor network switch 154 is coupled to neighboring processor network switches in other processor nodes, Fig. 1, para [0036]).

Regarding claim 9, Gonzalez teaches wherein: said array of processors comprises at least one interior processor with four adjacent neighboring processors (the array of processor nodes 140 is a four by four array of processor nodes 150, Fig. 1, para [0034]).

Regarding claim 10, Gonzalez teaches wherein: said array of processors comprises at least one processor situated on the perimeter of said array, and wherein said at least one processor further comprises a connection to an input/output (I/O) pin and further comprises an input/output (I/O) status bit (processors on the edges of the array may have links to processors and links to standard I/O devices, Fig. 1, para [0090], select between the input/output interface and the inter-processor interface based on a pin on the integrated circuit, para [0013]).

Regarding claim 11, Gonzalez teaches a method of sharing processing tasks between a plurality of processors, comprising: providing a first processor; providing a second processor (Fig. 1, para [0010]); providing a communication port between said first processor and said second processor (processor network interface 240 is a communication interface, Fig. 2, para [0041]); sending an input from said first processor to said second processor; and receiving said input by said second processor from said first processor, wherein said sending does not interrupt the processing functions of said second processor (information is communicated by message-passing among arrayed processor nodes, para [0060]).

Regarding claim 12, Gonzalez teaches wherein: said sending occurs when said second processor is executing a task (relationship among processes. Channels 640, 642 and 644 are shown for channeling data into and out from the processes underlying the kernels. The channels carry the results of each processor node, which is communicated to the next computational kernel for additional processing, Fig. 6, para [0068]).

- Please See Continuation Sheet -

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

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Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:
Box V.2. Citations and explanations:

Regarding claim 13, Gonzalez teaches wherein: said receiving is completed when said second processor temporarily pauses said executing and accepts said sending from said first processor (parent process updates input data for child process. When wait flag is cleared to zero, child process wakes up, Fig. 6, para [0072]).

Regarding claim 14, Gonzalez teaches wherein: said sending an input from said first processor further comprises setting an input flag bit high (wait flag is set, para [0072]).

Regarding claim 15, Gonzalez teaches wherein: responding to said received input by said second processor comprises executing code of said received input directly from said port (child process wakes up and starts executing their code, Fig. 6, para [0072]).

Regarding claim 16, Gonzalez teaches wherein: said executing code directly from said port is performed in the absence of storing said code to a memory location prior to said executing code directly (each of the child processes has access to the same program, data and/or variables, and thus can communicate among themselves. A parent process can update one or more data structures upon which child processes depend, Fig. 6, para [0072]).

Regarding claim 17, Gonzalez teaches a software program, wherein said software program comprises a step of temporarily pausing said executing a task of said second processor, and checking said port for potential input from said first processor (processing element 220 is a processor configured to execute applications. The processing element 220 includes a standard or native instruction set that provides a set of instructions that the processor element 220 is designed to recognize and execute, para [0039]).

Regarding claims 18 and 29, Gonzalez teaches a method, comprising: sending an input from a first processor to a second processor, wherein said second processor is inactive at time of said sending (parent process updates input data for child process. Wait flag is set to keep child process from executing (i.e. inactive but alert), Fig. 6, para [0072]); awakening said second processor to receive said input (child process wakes up and starts executing their code, Fig. 6, para [0072]); checking an input/output (I/O) register by said second processor to determine the source of said input (each processing node is associated with a unique node identifier or address by using a packet switched-like network to communicate information between at least two nodes by passing messages including such information, para [0060]); receiving said input by said second processor from said first processor; and responding to said input from said first processor by said second processor (processor network interface 240 receives a response packet, para [0043]).

Regarding claim 19, Gonzalez teaches wherein: said method is executed by a software loop (data cache 323 and instruction cache 324 are used to contain data and instructions, respectively, that the processing element 322 requires to perform its dedicated functionality, Fig. 3, para [0050]).

Regarding claim 20, Gonzalez teaches wherein: said awakening comprises a message header which is safe to throwaway after said awakening (data and instructions are communicated by message passing which includes a header, para [0060], processor network interface 240 strips the packet control information, para [0043]).

Regarding claim 21, Gonzalez teaches wherein: said checking comprises determining the status of read and write handshake status bits of adjacent processors (standard I/O interface 914 is an interface configured to handle standard I/O communication signals between chips or devices, Fig. 9, para [0085]).

Regarding claim 22, Gonzalez teaches wherein: said receiving is followed by lowering the read and write handshake status bits of said first processor and said second processor (standard I/O communication signals are communication signals that conform to commonly accepted industry or company standards, protocols, conventions, technology, or circuitry, Fig. 9, para [0085]).

Regarding claim 23, Gonzalez teaches wherein: said acting is followed by said second processor returning to an inactive mode (channels are established after the computational kernels are done executing. OS and other machine resources need only be involved in the creation of a channel and thereafter are not needed, para [0069]).

Regarding claim 24, Gonzalez teaches wherein: said awakening is caused by a multiple port read function (each of the child processes has access to the same program, data and variables, and thus can communicate among themselves. A parent process can update one or more data structures upon which child processes depend, para [0072]).

Regarding claim 25, Gonzalez teaches wherein: said awakening is caused by a pin (processors on the edges of the array may have links to processors and links to standard I/O devices, Fig. 1, para [0090], select between the input/output interface and the inter-processor interface based on a pin on the integrated circuit, para [0013]).

Regarding claim 26, Gonzalez teaches wherein: said receiving comprises reading said input as a data statement (processor network switch 327 allows data, instructions and other information to be communicated among an array of processing nodes, Fig. 3, para [0052]).

Regarding claim 27, Gonzalez teaches wherein: said method is located in ROM (processing element 220 is a processor configured to execute applications. The processing element 220 includes a standard or native instruction set that provides a set of instructions that the processor element 220 is designed to recognize and execute. These standard instructions are hard-coded into the silicon and cannot be modified, para [0039]).

- Please See Next Sheet -

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

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Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:
Box V.2. Citations and explanations:

Regarding claim 28, Gonzalez teaches wherein: said method is part of a boot up task in ROM (reset sequence mode, para [0071]).

Regarding claim 30, Gonzalez teaches a method for communicating between a plurality of computer processors, comprising: providing a first processor; providing a second processor, wherein said second processor is in an alert but inactive status (parent process updates input data for child process. Wait flag is set to keep child process from executing (i.e. inactive), Fig. 6, para [0072]); providing an I/O register for each of said plurality of computer processors (processor network interface 240 passes data to or from a memory mapped interface to read or write, para [0043]); sending an input from said first processor to said second processor, wherein said sending causes said second processor to change to an active status (parent process updates input data for child process. When wait flag is cleared to zero, child process wakes up, Fig. 6, para [0072]); reading the I/O register of said second processor to determine from which processor said input was sent (each processing node is associated with a unique node identifier or address by using a packet switched-like network to communicate information between at least two nodes by passing messages including such information, para [0060]); and directly executing said input by said second processor (child process wakes up and starts executing their code, Fig. 6, para [0072]).

Regarding claim 31, Gonzalez teaches reading said I/O register of said second processor an additional number of times to determine if additional inputs have been sent to said second processor; and executing said additional inputs by said second processor (data passing using software channels to send a stream of data from source to destination, para [0044]).

Regarding claim 32, Gonzalez teaches wherein: said additional inputs were sent from a third processor (processor network interface 240 receives data through the processor network switch 250 from the network of the array of processor nodes 140, and the processor network interface 240 transfers the data to the processing element 220 (i.e. input can come from any processor in the array), Fig. 1, para [0041]).

Regarding claim 33, Gonzalez teaches a processing system, comprising: an array of interconnected computer processors, wherein each processor further comprises: an I/O register (processor network interface 240 passes data to or from a memory mapped interface to read or write, para [0043]); a communication port located on each of four sides of said processors (processor network interface 240 is a communication interface, Fig. 2, para [0041]; the array of processor nodes 140 is a four by four array of processor nodes 150, Fig. 1, para [0034]); a sending mechanism for sending an input to other said processors; and a receiving mechanism for receiving an input from other said processors (information is communicated by message-passing among arrayed processor nodes, para [0060]); a monitoring mechanism in which each of said processors receiving said input can determine the source of said input (each processing node is associated with a unique node identifier or address by using a packet switched-like network to communicate information between at least two nodes by passing messages including such information, para [0060]); and an executing mechanism in which each of said processors receiving said input can respond to said input (processor network interface 240 receives a response packet, para [0043]).

Regarding claim 34, Gonzalez teaches wherein: said sending mechanism comprises a first port on a first processor sending the input, said first port being located adjacent to an intended receiving processor; and said receiving mechanism comprises a second port on said intended receiving processor, said second port being located adjacent to said first processor (Fig. 3, para [0048]-[0049]).

Regarding claim 35, Gonzalez teaches wherein: said receiving mechanism further comprises a latching mechanism to receive said input directly from said first port to said second port (read/write port is reserved for interacting with either the processor network switch 327, a local memory of a neighbor processor node or the processing element 322. Local memory 326 is designed to share data with other processor nodes, local memories and/or processing elements, Fig. 3, para [0056]-[0057]).

Regarding claim 36, Gonzalez teaches wherein: said monitoring mechanism of a first processor can suspend an active executing task of said first processor in order to determine if an input is attempting to be sent by a second processor (parent process updates input data for child process. Wait flag is set to keep child process from executing (i.e. suspended). When wait flag is cleared to zero, child process wakes up, Fig. 6, para [0072]).

Regarding claim 37, Gonzalez teaches wherein: said input is received by a receiving processor directly from a port of a sending processor (read/write port is reserved for interacting with either the processor network switch 327, a local memory of a neighbor processor node or the processing element 322. Local memory 326 is designed to share data with other processor nodes, local memories and/or processing elements, Fig. 3, para [0056]-[0057]).

Regarding claim 38, Gonzalez teaches wherein: said sending mechanism has the ability to send said input from one processor to a non-adjacent receiving processor (communications between a transmitting processor node 410 and the non-adjacent receiving processor node 320, Fig. 4, para [0058]).

Claims 1-38 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used in industry.

Form PCT/ISA/237 (Supplemental Box) (April 2007)